(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 803 812 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
31.07.2002 Bulletin 2002/31

(51) Int Cl.[7]: **G06F 11/14**

(21) Application number: **97106479.5**

(22) Date of filing: **18.04.1997**

(54) **Method and apparatus for updating a program**

Verfahren und Vorrichtung zur Aktualisierung eines Programms

Méthode et dispositif de mise à jour d'un programme

(84) Designated Contracting States:
DE FR GB

(30) Priority: **24.04.1996 JP 10220496**

(43) Date of publication of application:
29.10.1997 Bulletin 1997/44

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(56) References cited:
US-A- 5 432 927

- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 38, no. 7, July 1995, NEW YORK US, page 551 XP000521789 "Recovery Method for Damaged Firmware"**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an information processor, a method of updating a program and an information processing system and, more particularly, to an information processor, a program updating method and an information processing system suitable for updating a program such as a basic input/output system (BIOS) via a network.

2. Description of the Related Art

[0002] Networks of a kind represented by the Internet have been developed, to which network users can connect personal computers or the like to obtain various kinds of information.

[0003] A connection to the Internet or the like can be made through a communication network such as an analog telephone network or the Integrated Services Digital Network (ISDN). Recently, it has become possible to gain access to networks including the Internet through cables of a cable television (CATV) system.

[0004] For access to a network such as the Internet, an information processor having a transmitting and receiving circuit for transmission and reception through a predetermined communication network is used.

[0005] Fig. 9 shows an example of such an information processor using a modem 105 and capable of transmission and reception through an analog telephone circuit. A central processing unit (CPU) 101 executes various processings in accordance with programs stored in a flash electrically erasable programmable ROM (hereinafter referred to simply as "flash ROM") 102. Necessary data for execution of various processings performed by the CPU 101 and other data are suitably stored in a RAM 103. The CPU 101 receives data transmitted from the analog telephone circuit by using the modem 105. The CPU 101 processes the received data and displays, for example, received image data on a display unit (not shown) through a display interface 106.

[0006] A basic input/output system (BIOS), which is run by the CPU 101 when the processor is started up, and which is a basic program (a group of hardware-dependent control programs) for setting a configuration of the RAM 103 or initialization of a floppy disk drive 104, is stored in the flash ROM 102 as well as the programs for processing data supplied through the modem 105. The flash ROM 102 is an electrically erasable and programmable nonvolatile memory in which stored contents can be changed. The flash ROM 102 of such an erasable and programmable type is used to enable the BIOS to be updated according to a change in the specifications of units connected to the processor or according to updating of the operating system (OS) of the processor.

[0007] The BIOS in this information processor is updated as described below. First, a predetermined program for updating the BIOS is started and the BIOS stored in the flash ROM 102 is recorded on a floppy disk by the floppy disk drive 104. Thereafter, the floppy disk is taken out and another floppy disk on which a new BIOS is recorded is inserted into the floppy disk drive 104, and the new BIOS is stored in the flash ROM 102.

[0008] The step of recording the former BIOS on a floppy disk in this updating process is performed for the purpose of reinstalling the former BIOS if updating of the BIOS ends in failure, for example, if the floppy disk on which the new BIOS is recorded has such a defect that the new BIOS cannot be read out, or if the program of the new BIOS has a defect (bug) and cannot run normally.

[0009] However, BIOS updating is performed in a different manner in the case of an information processor having no floppy disk drive, e.g., a set top box (STB) used for access to a network such as the Internet through a cable of a CATV system. For example, in such an information processor, an external terminal unit is connected to a predetermined terminal provided in the information processor, and a BIOS is saved to the terminal unit before it is updated. For such BIOS updating, complicated operations are required.

[0010] US-A-5,432,927 relates to a loading system using separable EEPROM units (10 and 12) to facilitate safe reprogramming. When reprogramming (remapping) the new program is written into one of said units, the main memory. After checking that this new program is correct, the same new program is written also into the other of said units, the auxiliary memory, and is checked also. Thus after reprogramming the system has stored the (new) program double in both memories.

[0011] Further, IBM Technical Disclosure Bulletin, vol. 38, no. 7, July 1995, New York US, page 551, ref. XP 000521789, "Recovery Method for Damaged Firmware", discloses a flash memory system with a (normally) non-updateable portion containing a non-interactive program capable of restoring the flash to its operational state and with an updateable portion. In case of damaged firmware, a program in said non-updateable portion locates a file-based version thereof into a memory to restart the computer system. An updating procedure is not disclosed.

SUMMARY OF THE INVENTION

[0012] In view of the above-described circumstances, an object of the present invention is to provide an information processor, a program updating method and an information processing system arranged to save a current BIOS in a spare storage area before updating of the BIOS in order to enable the BIOS to be immediately reinstalled if writing of a new BIOS ends in failure and to prevent the old BIOS from being lost by an operation

error or the like.

[0013] To achieve the above-described object, according to one aspect of the present invention as recited in claim 1, there is provided an information processor comprising storage means having a main area in which a current basic program is stored, a common area in which an updating program describing a procedure for updating the basic program is stored, and a spare area in which the basic program is stored before it is updated, and processing means for performing updating on the basis of the updating program stored in the common area of the storage means, the updating including copying to the spare area the current basic program read out from the main area and finally writing a new basic program to the main area.

[0014] According to another object of the present invention, as recited in claim 7, there is provided a program updating method of updating a current basic program stored in a main area of storage means by replacing the current basic program with a new basic program on the basis of an updating program stored in a common area of the storage means, the method comprising the steps of copying to the spare area of the storage means the current basic program read out from the main area, and finally writing the new basic program to the main area on the basis of the updating program.

[0015] Further enhancements are provided by the subclaims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Fig. 1 is a diagram showing the configuration of an information providing system to which an information receiving system of the present invention is applied;

Fig. 2 is a diagram showing the configuration of an information processor in home 5-1 shown in Fig. 1;

Fig. 3 is a block diagram showing the internal configuration of home server 11 shown in Fig. 2;

Fig. 4 is a block diagram showing the internal configuration of personal computer 12-1 shown in Fig. 2;

Fig. 5 is a block diagram showing the internal configuration of STB 16 shown in Fig. 2;

Fig. 6 is a block diagram showing the internal configuration of flash ROM 91 shown in Fig. 5;

Figs. 7A and 7B are diagrams showing the relationship between a logical address space and a physical address space in flash ROM 91 shown in Fig. 5;

Fig. 8 is a flowchart showing the operation of STB 16 at the time of BIOS updating;

Fig. 9 is a block diagram showing an example of an information processor having a recording unit; and

Figs. 10 through 18 are diagram for explaining the operation of STB 16 at the time of BIOS updating.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Fig. 1 is a diagram showing the configuration of an information providing system which is an embodiment of the information processing system of the present invention. Servers 1-1 and 1-2 (information providing means) provide information consisting mainly of images and sounds accompanying the images or other kinds of data and relating to video on-demand (VOD) services to homes 5-1 to 5-6 through networks. As networks in this system, a cable television network 2, the Integrated Services Digital Network (ISDN) 3, an analog telephone circuit 4 are used.

[0018] For example, the server 1-1 provides information to a cable television center 2-1 or 2-2 through the cable television network 2. The cable television center 2-1 provides the provided information to the homes 5-1 and 5-2 of subscribers for the cable television system. Similarly, the cable television center 2-2 provides information to the homes 5-1, 5-3, and 5-4 of subscribers for the corresponding cable television system.

[0019] The server 1-1 also provides information through the ISDN 3 or the analog telephone circuit 4. From each of the homes 5-1 to 5-6, the server 1-1 can be accessed through the ISDN 3 or the analog telephone circuit 4, and each home can be provided with information through this network or circuit.

[0020] The server 1-2 also provides various kinds of information to the homes 5-1 to 5-6, as does the server 1-1.

[0021] This video transmission system may be such that trunks corresponding to transmission channels are formed of optical fibers, optical fiber nodes covering 300 to 500 homes are provided, and hybrid fiber coaxes (HFCs), i.e., coaxial cable for information transmission are used between the optical fiber nodes and the homes. Alternatively, a fiber-to-the-curve (FTTC) system may be formed in which information is transmitted to a pedestal (repeater) covering 24 homes or so, i.e., a vicinal area about one home through an optical fiber and is transmitted form the pedestal to each home through a coaxial cable, or a fiber-to-the-home (FTTH) system may be formed in which information is transmitted to homes through optical fibers.

[0022] In the embodiment shown in Fig. 1, the transmission capacity of the cable television network 2 is larger than that of the ISDN 3, which is larger than that of the analog telephone circuit 4. Accordingly, if the cable television network 2 is used, moving images highest in quality and in moving speed can be received in a real time manner at each home. In the case of using the ISDN 3, ordinary moving images, which do not move so quickly as those receivable through the cable television network 2, can be received in a real time manner. However, moving images cannot be received in a real time manner through the ISDN 3 if they move at an excessively high speed. In contrast, in the case of using the analog telephone circuit 4, moving images cannot be re-

ceived and only still images can be received since the transmission capacity is small. Audio signals can be received in a real time manner by using each of the above-described networks.

[0023] Fig. 2 shows the configuration of an information receiving system provided in the home 5-1. Information processing systems (not shown) which are basically the same as that provided in the home 5-1 are also provided in the other homes.

[0024] A home server 11 connects to the cable television network 2, the ISDN 3 and the analog telephone circuit 4 and connects at least one of these networks to a personal computer 12-1, a personal computer 12-2, an STB 16 (information processing means) or a telephone set 18.

[0025] A keyboard 14-1 and a mouse 15-1 are connected to the personal computer 12-1 to input various instructions. Images output from the personal computer 12-1 as desired are displayed on a display unit 13-1.

[0026] Similarly, a keyboard 14-2 and a mouse 15-2, and a display 13-2 are connected to the personal computer 12-2.

[0027] The STB 16 receives image data supplied from the home server 11, demodulates the received image data and outputs the demodulated data to a television receiver 17 to display corresponding images. The STB 16 is also used for a video on-demand (VOD) service for providing programs in response to user's requests. The telephone set 18 enables telephonic communication through the home server 11.

[0028] Fig. 3 shows the configuration of components of the home server 11. A CPU 31 executes various processings in accordance with programs stored in a ROM 32. Necessary data for execution of various processings performed by the CPU 31 and other data are suitably stored in a RAM 33. A hard disk drive 34 records information on its internal hard disk and reproduces information from the hard disk.

[0029] The home server 11 has various interfaces. Each of network interfaces 35 to 37 interfaces with the cable television network 2, the ISDN 3 or the analog telephone circuit 4 for data exchange with the same. An STB interface 38 interfaces with the STB 16 in an asynchronous transfer mode (ATM). A computer interface 39 is connected to the personal computer 12-1 and interfaces for Ethernet communication. A computer interface 40 is connected to the personal computer 12-2 and interfaces in accordance with special protocols for the personal computer 12-2. A telephone interface 41 interfaces with the telephone set 18.

[0030] Fig. 4 shows the configuration of components of the personal computer 12-1. A CPU 71 executes various processings in accordance with programs stored in a ROM 72. Necessary data for execution of various processings performed by the CPU 71 and other data are suitably stored in a RAM 73. A hard disk drive 74 records information on its internal hard disk and reproduces information from the hard disk. A floppy disk drive 75 executes processing for recording information on a floppy disk or reproducing information from a floppy disk.

[0031] A home server interface 76 interfaces with the home server 11. A keyboard interface 77 and a mouse interface 78 interface with the keyboard 14-1 and the mouse 15-1, respectively. A display interface 79 interfaces with the display 13-1.

[0032] The personal computer 12-2 is constructed in the same manner as the personal computer 12-1.

[0033] Fig. 5 shows the configuration of components of the STB 16, which is an information processor, and which represents an embodiment the present invention. A CPU 51 (processing means) executes various processings in accordance with programs stored in a flash ROM 91 (storage means) mounted on a flash ROM board 52. Necessary data for execution of various processings performed by the CPU 51 and other data are suitably stored in a RAM 53. A graphic controller 54 is supplied with graphic data from the CPU 51 and outputs the graphic data to the television receiver 17 to display the data. A Moving Picture Experts Group (MPEG) 2 video decoder 55 and an MPEG audio decoder 56 respectively decode video data and audio data supplied from the home server 11 through a network interface card 57 (receiving means) by MPEG 2 and MPEG systems, and output the decoded data to the television receiver 17 to display images and to radiate sounds.

[0034] The network interface card 57 is connected between the STB 16 and the home server 11 to interface with the home server 11. A smart card interface 58 interfaces with a smart card 59, which is detachably attached to the STB 16 when necessary. Personal information of the card user, key information for scrambling data, accounting information and the like are stored in the smart card 59.

[0035] A joystick interface 60 interfaces with a game machine 61 connected to the STB 16. An infrared ray (IR) remote commander interface 62 receives an infrared ray (IR) signal from a remote commander 63 and outputs a corresponding command to the CPU 51.

[0036] A BIOS (a group of hardware-dependent control programs in the operating system run by the CPU 51), which is a group of basic programs run by the CPU 51 at the time of a start-up of the information processor to set a configuration of RAM 53 and to control data exchange with an external unit such as game machine 61, is stored in the flash ROM 91 mounted on the flash ROM board 52 along with the programs for processing data supplied through the network interface card 57. The flash ROM 91 on the flash ROM board 52 is an electrically erasable and programmable nonvolatile memory in which stored contents can be changed, and which maintains stored contents even after turning-off of the power supply. The flash ROM 91 of such an electrically erasable and programmable type is used to enable the BIOS to be updated according to one's need. A new BIOS is transmitted from the server 1-1 or server 1-2 to

be supplied to the STB 16 through a predetermined communication circuit and through the home 'server 11 and is received by the network interface card 57 of the STB 16.

[0037] Fig. 6 shows the configuration of the flash ROM board 52. The flash ROM 91 is an erasable and programmable nonvolatile memory for storing data in the program form and other data. The flash ROM 91 is used as two banks: a bank A 91a (main area) and a bank B 91b (spare area). The bank A 91a and the bank B 91b are used as one logical address space by the CPU 51. That is, as shown in Fig. 7A, two physical address spaces (bank A 91a and bank B 91b) are allotted in one logical address space. Contents (data such as programs) (Fig. 7B) stored in the bank A 91a or contents (Fig. 7C) stored in the bank B 91b are read out according to the bank changing operation of a bank change circuit 92. Also, in the case of storing (writing) data such as a program, the data is stored (written) in the bank A 91a or bank B 91b according to the bank changing operation of the bank change circuit 92. The bank change circuit 92 is circuit for converting a logical address addressed by the CPU 51 into an actual physical address in the flash ROM 91 (bank A 91a or bank B 91b).

[0038] The bank A 91a of the flash ROM 91 stores a program such as a current new BIOS while the bank B 91b stores a program such as a BIOS before updating (old version). A part of the flash ROM 91 is used as a common area 91c which can be accessed regardless of bank change. That is, the same storage area (physical address) is designated with a predetermined logical address regardless of bank change. In this area, data which is first read to the memory when the processor is started up and a BIOS updating program are stored and the contents of this area cannot be rewritten.

[0039] The bank change circuit 92 operates for changeover between the banks A and B in the memory 91 according to a value held by a bank state register 93 formed of a hardware logic circuit to store data such as a program in a storage area designated with addresses supplied via an address bus or to read out data from a storage area. Data to be stored or output is input or output through a data bus.

[0040] The bank state register 93 holds a value corresponding to one of the banks A and B which is to be used. This value is supplied from the CPU 51 via the bus. A BIOS and other programs ordinarily used are stored in the bank A. Therefore, the bank state register 93 is holding the value corresponding to the bank A except during a BIOS updating period. In this embodiment, when the power supply for the STB is turned on, the bank state register 93 is reset to the value corresponding to the bank A.

[0041] As described above, in the circuit on the flash ROM board 52, the bank A or bank B of the memory section 91 is used according to the value held by the bank state register 93, and data is read out mainly from the bank A except during a BIOS updating period.

[0042] The operation of this embodiment of the invention at the time of updating a BIOS in the flash ROM board 52 will next be described with reference to the flowchart of Fig. 8 and the diagrams of Fig. 10 to 18. In this embodiment, no unit for driving a portable recording medium such as a floppy disk is provided and, therefore, a new BIOS is supplied from the network interface card 57 for BIOS updating. When the remote commander 63 or the like (e.g., server 1-1 or 1-2 as shown in Fig. 1) is operated to input an instruction to perform BIOS updating, the CPU 51 starts processing described below on the basis of the updating program stored in the common area 91c.

[0043] First, in step S1, the CPU 51 reads out a current version BIOS which is to be updated, and which has been stored in the bank A 91a of the flash ROM 91, and the CPU 51 temporarily stores (saves) the current BIOS in the RAM 53, as shown in Fig. 10.

[0044] Next, in step S2, the CPU 51 changes the value of the bank state register 93 to change the bank A for the bank B.

[0045] In step S3, the CPU 51 erases the contents, i. e., an old version BIOS, in the bank B of the flash ROM 91, as shown in Fig. 11. In step S4, the CPU 51 reads out the current version BIOS from the RAM 53 and stores the current version BIOS in the bank B 91b, as shown in Fig. 12.

[0046] In step S5, the CPU 51 collates the current BIOS in the bank B 91b of the flash ROM 91 with the current BIOS in the RAM 53, as shown in Fig. 13. In step S6, the CPU 51 makes a determination as to whether these two groups of memory contents are identical with each other. If NO, the CPU 51 returns the process to step S1 to again execute the operation of moving the BIOS stored in the bank A 91a of the flash ROM 91 to the bank B 91b via the RAM 53.

[0047] If the CPU 51 determines in step S6 that the two groups of BIOS data in the RAM 53 and the bank B 91b of the flash ROM 91 are identical with each other, it moves the process to step S8 to change the value of the bank state register 93, thereby changing the bank B for the bank A.

[0048] Next, in step S9, the network interface card 57 receives a new BIOS supplied via a predetermined communication network and the home server 11, and the CPU 51 stores in the RAM 53 the new BIOS received by the network interface card 57, as shown in Fig. 14.

[0049] In step S10, the CPU 51 erases the contents (current BIOS) of the bank A of the flash ROM 91, as shown in Fig. 15. Thereafter, in step S11, the CPU 51 stores in the bank A 91a of the flash ROM 91 the new BIOS which is stored in the RAM 53, as shown in Fig. 16.

[0050] In step S12, the CPU 51 collates the BIOS in the bank A 91a of the flash ROM 91 with the BIOS in the RAM 53, as shown in Fig. 17. In step S13, the CPU 51 makes a determination as to whether these two groups of memory contents are identical with each other. If NO, the CPU 51 returns the process to step S9 to

again perform the operation of moving the new BIOS stored in the RAM 53 to the bank A 91a of the flash ROM 91.

[0051] If the CPU 51 determines in step S13 that the two groups of BIOS data in the RAM 53 and the bank A 91a of the flash ROM 91 are identical with each other, it stops BIOS update processing with an update processing result shown in Fig. 18.

[0052] As described above, an old BIOS in the bank A 91a of the flash ROM 91 is moved to the bank B 91b in steps S1 to S7, and a new BIOS supplied via a predetermined communication network is stored in the bank A 91a in steps S8 to S13, thus performing BIOS updating. If the new BIOS does not run well, a sequence of operations reverse to that shown as steps S1 to S7 is performed to move the BIOS in the bank 91b of the flash ROM 91 to the bank A 91a via the RAM 53, thereby reinstalling the former BIOS.

[0053] While in the above-described embodiment the flash ROM 91 having a plurality of banks is used, a plurality of flash ROMs each having a single storage area may be used in place of the flash ROM 91.

[0054] Any program (e.g., an operating system) other than the BIOS described above as an updated program may also be updated in accordance with the present invention. Further, flash ROMs may also be used in the home server 11, the personal computers 12-1 and 12-2 and other components.

[0055] In the information processor and the program updating method of the present invention for updating a current basic program stored in a main area of storage means by replacing the current basic program with a new basic program on the basis of an updating program stored in a common area of the storage means, the current basic program read out from the main area is copied to the spare area of the storage means, and the new basic program is finally written to the main area on the basis of the updating program. Thus, BIOS updating can be performed after saving an old BIOS to a spare area even in an apparatus having no such a recording unit as a floppy disk. Even in a case where BIOS writing ends in failure, the old BIOS can be reinstalled immediately, thus preventing the BIOS from being lost by an operation error or the like.

[0056] The information processing system of the present invention has information providing means for providing information through a predetermined transmission channel, and information processing means for performing updating on the basis of an updating program stored in a common area of storage means. This updating includes copying to a spare area of the storage means a current basic program read out from a main area of the storage means and finally writing to the main area of the storage means a new basic program supplied through the transmission channel. If such a system is used, BIOS updating can be performed by using a new BIOS supplied through a network line such as a transmission channel after saving an old BIOS to a spare area even in an apparatus having no such a recording unit as a floppy disk.

Claims

1. An information processor comprising:

   storage means (91) having a main area (91a) in which a current basic program is stored, a common area (91c) in which an updating program describing a procedure for updating the basic program is stored, and a spare area (91b) in which the basic program is stored before it is updated; and
   processing means (51) for performing updating on the basis of the updating program stored in the common area (91c) of said storage means, said updating including copying to said spare area (91b) the current basic program read out from said main area (91a) and finally writing a new basic program to said main area (91a).

2. An information processor according to Claim 1, wherein said basic program comprises a basic input/output system which is a group of hardware-dependent control programs.

3. An information processor according to Claim 1 or 2, further comprising receiving means for receiving information supplied through a predetermined transmission channel, said receiving means receiving a new basic program as said information through the transmission channel, said processing means (51) performing updating on the basis of the updating program stored in the common area of said storage means, said updating including copying to the spare area of said storage means the current basic program read out from the main area of said storage means and finally writing the new basic program received by said receiving means to the main area of said storage means.

4. An information processor according to Claim 3, wherein said receiving means receives information about video on-demand service through said transmission channel.

5. An information processor according to anyone of the preceding Claims, wherein said storage means (91) is formed of an electrically erasable and programmable read-only memory (52).

6. An information processor according to Claim 5, wherein the main and spare areas of said storage means (91) are allotted as separate banks in one logical address space, and one of the banks is alternatively selected by bank changing to be ad-

dressed.

7. The information processor of anyone of claims 1 to 6, wherein

information providing means provide information through a predetermined transmission channel (1, 2, 3, 4, 5, 11, 57) and
said processing means (51) perform said updating on the basis of a new program also received via said transmission channel.

8. A program updating method of updating a current basic program stored in a main area (91a) of storage means (91) by replacing the current basic program with a new basic program on the basis of an updating program stored in a common area (91c) of the storage means (91), said method comprising the steps of:

copying to a spare area (91b) of the storage means (91) the current basic program read out from the main area (91a); and
finally writing the new basic program to the main area (91a) on the basis of the updating program.

9. The program updating method of claim 8, wherein the copying step comprises

saving to a temporary storage area the current basic program read out from the main area (91a);
writing the current basic program saved to the temporary storage area to a spare area (91b) of the storage means (91);
collating the current basic program written to the spare area (91b) of the storage means (91) with the current basic program saved to the temporary storage area, and wherein the finally writing step comprises

writing to the temporary storage area a new basic program supplied from the outside and thereafter writing the new basic program to the main area (91a) of the storage means (91); and
collating the new basic program written to the main area (91a) of the storage means (91) with the new basic program written to the temporary storage area.

Patentansprüche

1. Informationsprozessor, umfassend
eine Speichereinrichtung (91) mit einem Hauptbereich (91a), in welchem ein aktuelles Grundprogramm gespeichert ist, einem gemeinsamen Bereich (91c), in welchem ein Aktualisierungsprogramm gespeichert ist, welches eine Prozedur zur Aktualisierung des Grundprogramms beschreibt, und einem Reservebereich (91b), in den das Grundprogramm gespeichert wird, bevor es aktualisiert wird,
und eine Verarbeitungseinrichtung (51) zur Ausführung einer Aktualisierung auf der Grundlage des in dem gemeinsamen Bereich (91c) der genannten Speichereinrichtung gespeicherten Aktualisierungsprogramms, wobei die betreffende Aktualisierung ein Kopieren des aus dem genannten Hauptbereich (91a) ausgelesenen aktuellen Grundprogramms in den genannten Reservebereich (91b) und schließlich ein Schreiben eines neuen Grundprogramms in den betreffenden Hauptbereich (91a) umfasst.

2. Informationsprozessor nach Anspruch 1, wobei das genannte Grundprogramm ein Grund-Eingabe-/Ausgabesystem aufweist, welches eine Gruppe von hardwareabhängigen Steuerprogrammen ist.

3. Informationsprozessor nach Anspruch 1 oder 2, umfassend ferner eine Empfangseinrichtung für den Empfang einer Information, die über einen bestimmten Übertragungskanal zugeführt wird,
wobei die betreffende Empfangseinrichtung ein neues Grundprogramm als die genannte Information über den Übertragungskanal empfängt,
wobei die genannte Verarbeitungseinrichtung (51) eine Aktualisierung auf der Grundlage des in dem gemeinsamen Bereich der genannten Speichereinrichtung gespeicherten Aktualisierungsprogramms ausführt,
wobei die betreffende Aktualisierung das Kopieren des aus dem Hauptbereich der genannten Speichereinrichtung ausgelesenen aktuellen Grundprogramms in den Reservebereich der betreffenden Speichereinrichtung und schließlich das Schreiben des durch die genannte Empfangseinrichtung empfangenen neuen Grundprogramms in den Hauptbereich der genannten Speichereinrichtung umfasst.

4. Informationsprozessor nach Anspruch 3, wobei die genannte Empfangseinrichtung eine Information über einen Video-bei-Bedarf-(Video-on-demand) -Service über den genannten Übertragungskanal empfängt.

5. Informationsprozessor nach einem der vorhergehenden Ansprüche, wobei die genannte Speichereinrichtung (91) aus einem elektrisch löschbaren und programmierbaren Festspeicher (52) gebildet ist.

6. Informationsprozessor nach Anspruch 5, wobei die

Hauptund Reservebereiche der genannten Speichereinrichtung (91) als gesonderte Banken in einem logischen Adressenraum bestimmt werden und wobei eine der Banken durch einen zu adressierenden Bankwechsel abwechselnd ausgewählt wird.

7. Informationsprozessor nach einem der Ansprüche 1 bis 6,
wobei Informationsbereitstellungseinrichtungen Informationen über einen bestimmten Übertragungskanal (1, 2, 3, 4, 5, 11, 57) bereitstellen
und wobei die genannte Verarbeitungseinrichtung (51) die genannte Aktualisierung auf der Grundlage eines ebenfalls über den genannten Übertragungskanal empfangenen neuen Programms ausführt.

8. Programmaktualisierungsverfahren zur Aktualisierung eines aktuellen Grundprogramms, welches in einem Hauptbereich (91a) einer Speichereinrichtung (91) gespeichert ist, durch Ersetzen des aktuellen Grundprogramms durch ein neues Grundprogramm auf der Grundlage eines in einem gemeinsamen Bereich (91c) der Speichereinrichtung (91) gespeicherten Aktualisierungsprogramms, umfassend die Verfahrensschritte:

Kopieren des aus dem Hauptbereich (91a) ausgelesenen aktuellen Grundprogramms in einen Reservebereich (91b) der Speichereinrichtung (91)
und schließlich Einschreiben des neuen Grundprogramms in den Hauptbereich (91a) auf der Grundlage des Aktualisierungsprogramms.

9. Programmaktualisierungsverfahren nach Anspruch 8, wobei der Kopierschritt das Sichern des aus dem Hauptbereich (91a) ausgelesenen aktuellen Grundprogramms in einem Zwischenspeicherbereich, das Schreiben des in dem Zwischenspeicherbereich gesicherten aktuellen Grundprogramms in einen Reservebereich (91b) der Speichereinrichtung (91) und das Vergleichen des in den Reservebereich (91b) der Speichereinrichtung (91) eingeschriebenen aktuellen Grundprogramms mit dem in dem Zwischenspeicherbereich gesicherten aktuellen Grundprogramm umfasst, und wobei der schließlich erfolgende Schreibschritt das Schreiben eines von außen her zugeführten neuen Grundprogramms in den Zwischenspeicherbereich und danach das Schreiben des neuen Grundprogramms in den Hauptbereich (91a) der Speichereinrichtung (91) und das Vergleichen des in den Hauptbereich (91a) der Speichereinrichtung (91) eingeschriebenen neuen Grundprogramms mit dem in den Zwischenspeicherbereich eingeschriebenen neuen Grundprogramm umfasst.

Revendications

1. Processeur d'information comprenant :

un moyen (91) de mémorisation comportant une zone principale (91a) dans laquelle est mémorisé un programme de base courant, une zone commune (91c) dans laquelle est mémorisé un programme de mise à jour décrivant une procédure destinée à mettre à jour le programme de base, et une zone (91 b) de réserve dans laquelle est mémorisé le programme de base avant qu'il soit mis à jour ; et
un moyen (51) de traitement destiné à effectuer la mise à jour sur la base du programme de mise à jour mémorisé dans la zone commune (91c) dudit moyen de mémorisation, ladite mise à jour incluant la copie, vers ladite zone (91b) de réserve, du programme de base courant lu dans ladite zone principale (91a) et finalement l'écriture d'un nouveau programme de base dans ladite zone principale (91a).

2. Processeur d'information selon la revendication 1, dans lequel ledit programme de base comprend un système d'entrée/sortie de base qui est un groupe de programmes de commande dépendant du matériel.

3. Processeur d'information selon la revendication 1 ou 2, comprenant en outre un moyen de réception destiné à recevoir de l'information délivrée par une voie de transmission prédéterminée, ledit moyen de réception recevant un nouveau programme de base en tant que ladite information par la voie de transmission, ledit moyen (51) de traitement effectuant la mise à jour sur la base du programme mis à jour mémorisé dans la zone commune dudit moyen de mémorisation, ladite mise à jour incluant la copie, vers la zone de réserve dudit moyen de mémorisation, du programme de base courant lu dans ladite zone principale dudit moyen de mémorisation et, finalement, l'écriture du nouveau programme de base, reçu par ledit moyen de réception, dans ladite zone principale dudit moyen de mémorisation.

4. Processeur d'information selon la revendication 3, dans lequel ledit moyen de réception reçoit, par ladite voie de transmission, de l'information au sujet d'un service de vidéo à la demande.

5. Processeur d'information selon l'une quelconque des revendications précédentes, dans lequel ledit moyen (91) de mémorisation et constitué d'une mémoire morte effaçable et programmable électriquement (52).

6. Processeur d'information selon la revendication 5,

dans lequel lesdites zones principale et de réserve dudit moyen (91) de mémorisation sont affectées en tant que rangées distinctes dans un espace d'adresses logiques, et dans lequel l'une des rangées est choisie alternativement par changement de la rangée à adresser.

7. Processeur d'information selon l'une quelconque des revendications 1 à 6, dans lequel :

le moyen de fourniture d'information foumit de l'information par une voie (1, 2, 3, 4, 5, 11, 57) de transmission prédéterminée ; et
ledit moyen (51) de traitement effectue ladite mise à jour sur la base d'un nouveau programme reçu aussi par ladite voie de transmission.

8. Procédé de mise à jour de programme consistant à mettre à jour un programme de base courant mémorisé dans une zone principale (91a) d'un moyen (91) de mémorisation par remplacement du programme de base courant par un nouveau programme de base sur la base d'un programme de mise à jour mémorisé dans une zone commune (91c) du moyen (91) de mémorisation, ledit procédé comprenant les étapes consistant :

à copier, vers une zone (91b) de réserve dudit moyen (91) de mémorisation, le programme de base courant lu dans la zone principale (91a) ; et
à écrire finalement le nouveau programme de base dans la zone principale (91a) sur la base du programme de mise à jour.

9. Procédé de mise à jour de programme selon la revendication 8, dans lequel l'étape de copie comprend :

la sauvegarde, vers une zone de mémorisation temporaire, du programme de base courant lu dans la zone principale (91a) ;
l'écriture du programme de base courant, sauvegardé dans la zone de mémorisation temporaire, dans une zone (91b) de réserve du moyen (91) de mémorisation ;
la fusion du programme de base courant, écrit dans la zone (91b) de réserve du moyen (91) de mémorisation, avec un programme de base courant sauvegardé vers la zone de mémorisation temporaire, et dans lequel l'étape d'écriture finale comprend :

l'écriture dans la zone de mémorisation temporaire d'un nouveau programme de base délivré de l'extérieur et l'écriture ensuite du nouveau programme de base dans la zone principale (91a) du moyen (91) de mémorisation ; et
la fusion du nouveau programme de base, écrit dans la zone principale (91 a) du moyen (91) de mémorisation, avec le nouveau programme de base écrit dans la zone de mémorisation temporaire.

FIG. 1

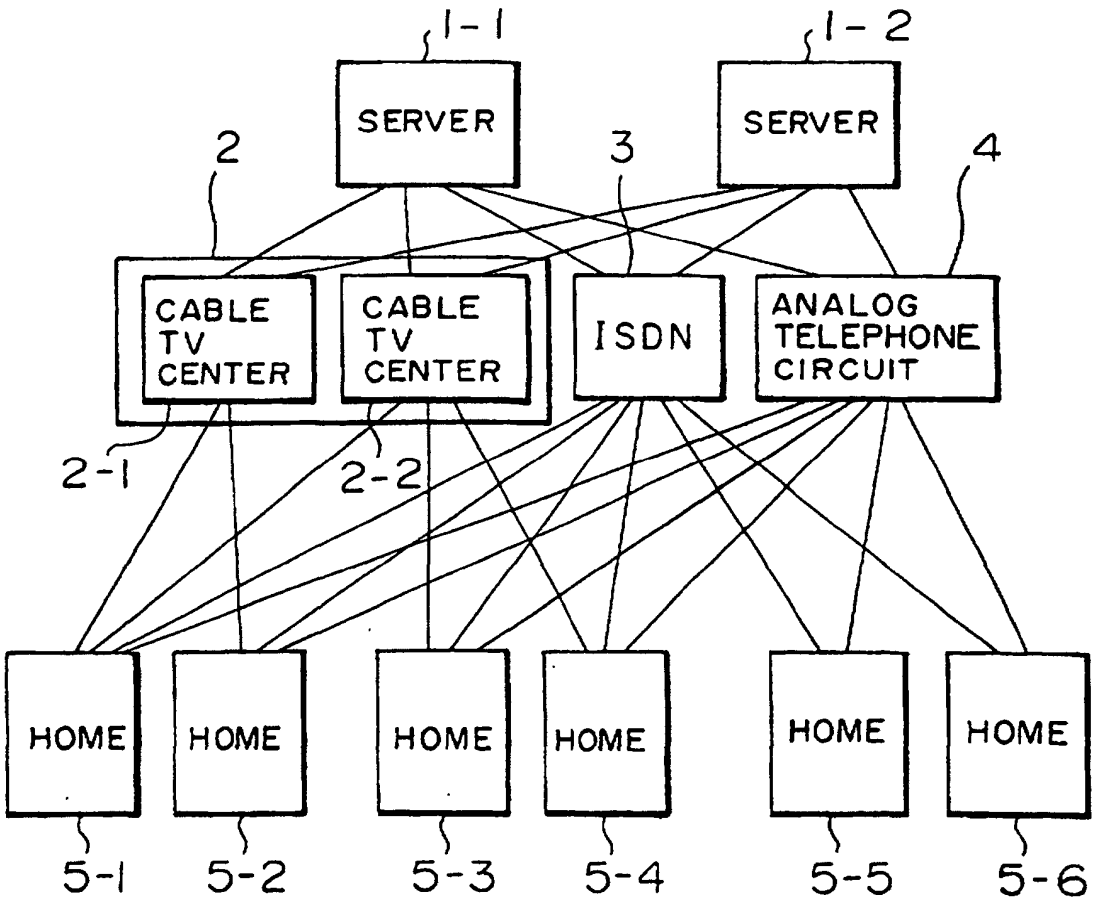

1-1
1-2
SERVER
SERVER
2
3
4
CABLE TV CENTER
CABLE TV CENTER
ISDN
ANALOG TELEPHONE CIRCUIT
2-1
2-2
HOME
HOME
HOME
HOME
HOME
HOME
5-1
5-2
5-3
5-4
5-5
5-6

FIG. 2

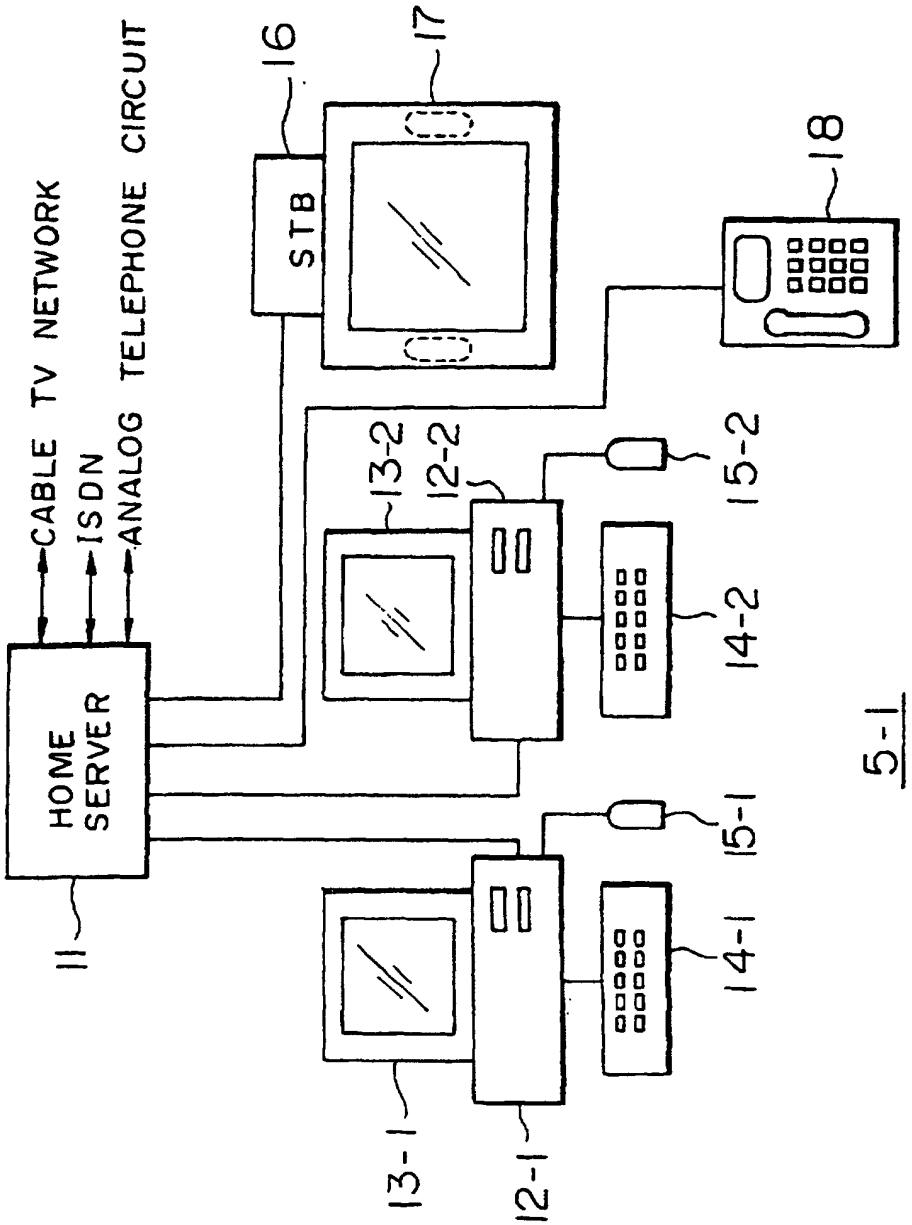

CABLE TV NETWORK
ISDN
ANALOG TELEPHONE CIRCUIT
HOME SERVER
11
STB
16
17
18
13-2
12-2
15-2
14-2
15-1
14-1
13-1
12-1
5-1

FIG. 3

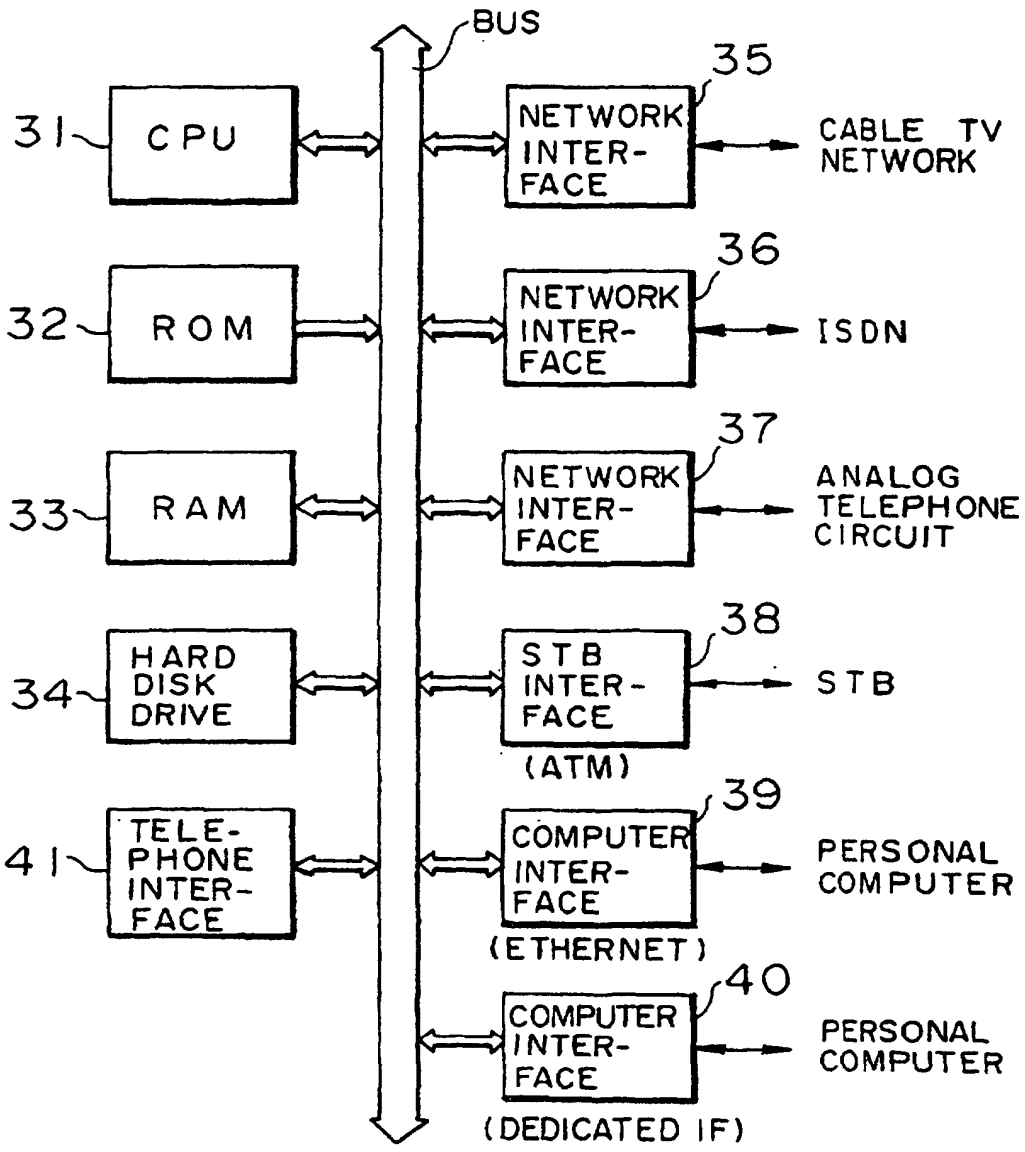

BUS
31
CPU
32
ROM
33
RAM
34
HARD DISK DRIVE
41
TELE-PHONE INTER-FACE
35
NETWORK INTER-FACE
CABLE TV NETWORK
36
NETWORK INTER-FACE
ISDN
37
NETWORK INTER-FACE
ANALOG TELEPHONE CIRCUIT
38
STB INTER-FACE
STB
(ATM)
39
COMPUTER INTER-FACE
PERSONAL COMPUTER
(ETHERNET)
40
COMPUTER INTER-FACE
PERSONAL COMPUTER
(DEDICATED IF)
11

FIG.4

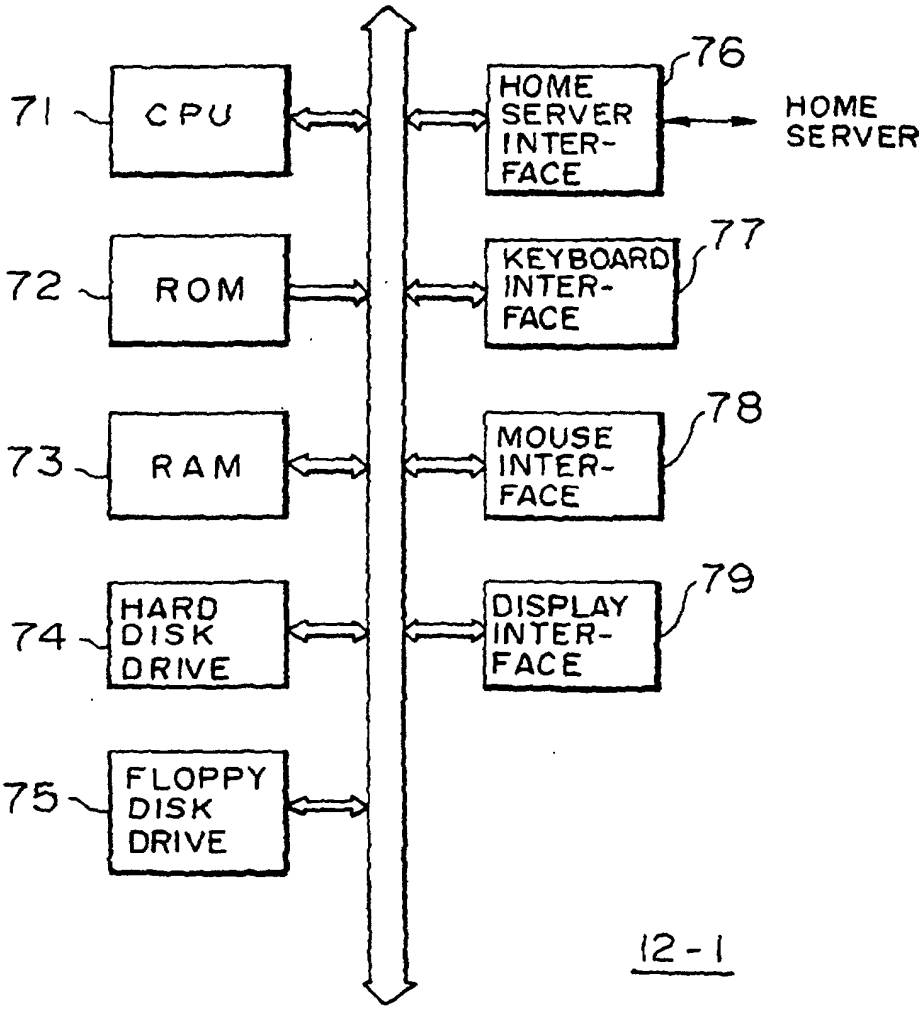
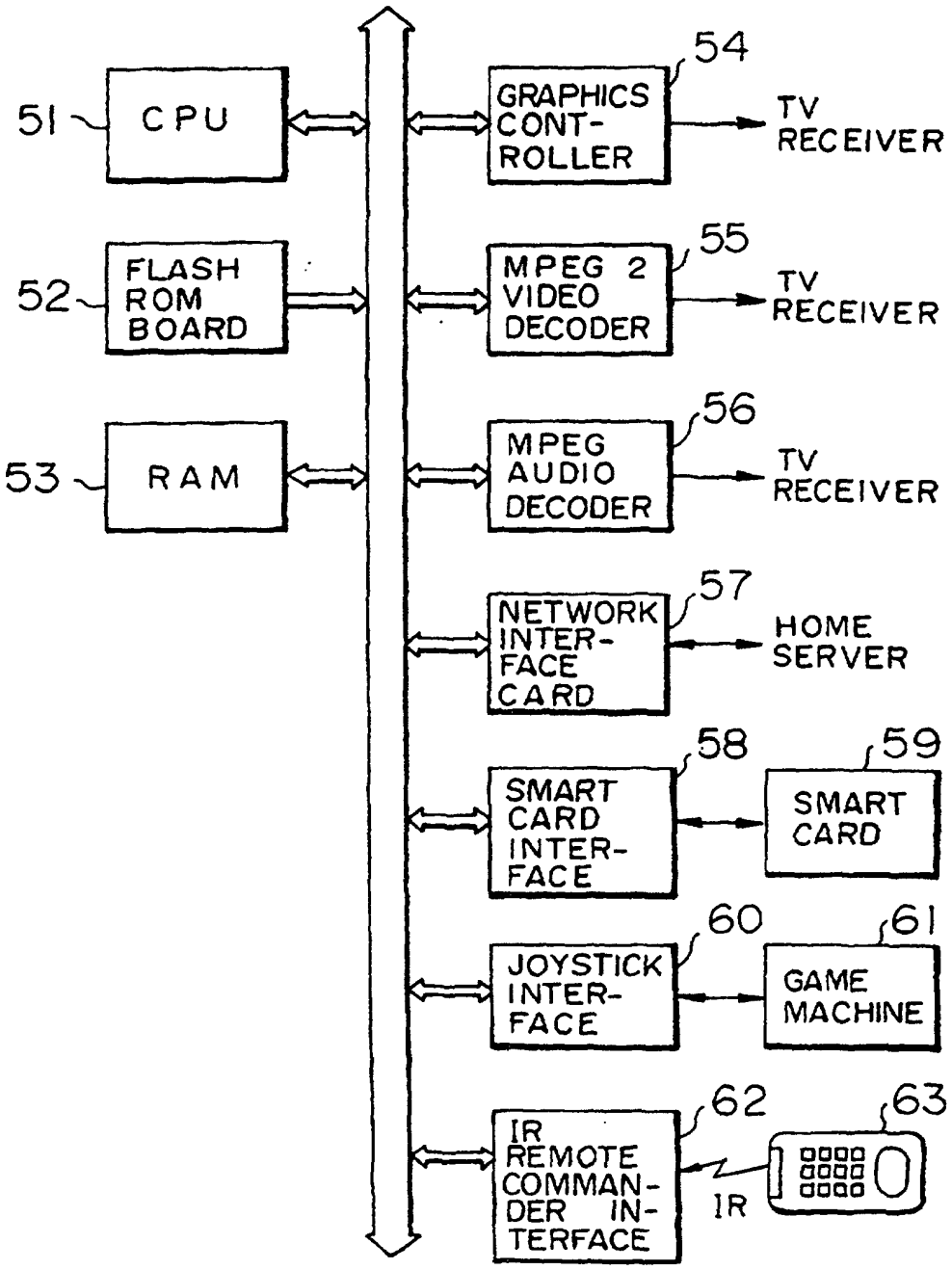

71
CPU
72
ROM
73
RAM
74
HARD DISK DRIVE
75
FLOPPY DISK DRIVE
76
HOME SERVER INTER-FACE
HOME SERVER
77
KEYBOARD INTER-FACE
78
MOUSE INTER-FACE
79
DISPLAY INTER-FACE
12-1

FIG. 5


51
CPU
52
FLASH ROM BOARD
53
RAM
54
GRAPHICS CONT-ROLLER
TV RECEIVER
55
MPEG 2 VIDEO DECODER
TV RECEIVER
56
MPEG AUDIO DECODER
TV RECEIVER
57
NETWORK INTER-FACE CARD
HOME SERVER
58
SMART CARD INTER-FACE
59
SMART CARD
60
JOYSTICK INTER-FACE
61
GAME MACHINE
62
IR REMOTE COMMAN-DER IN-TERFACE
63
IR

16

FIG. 6

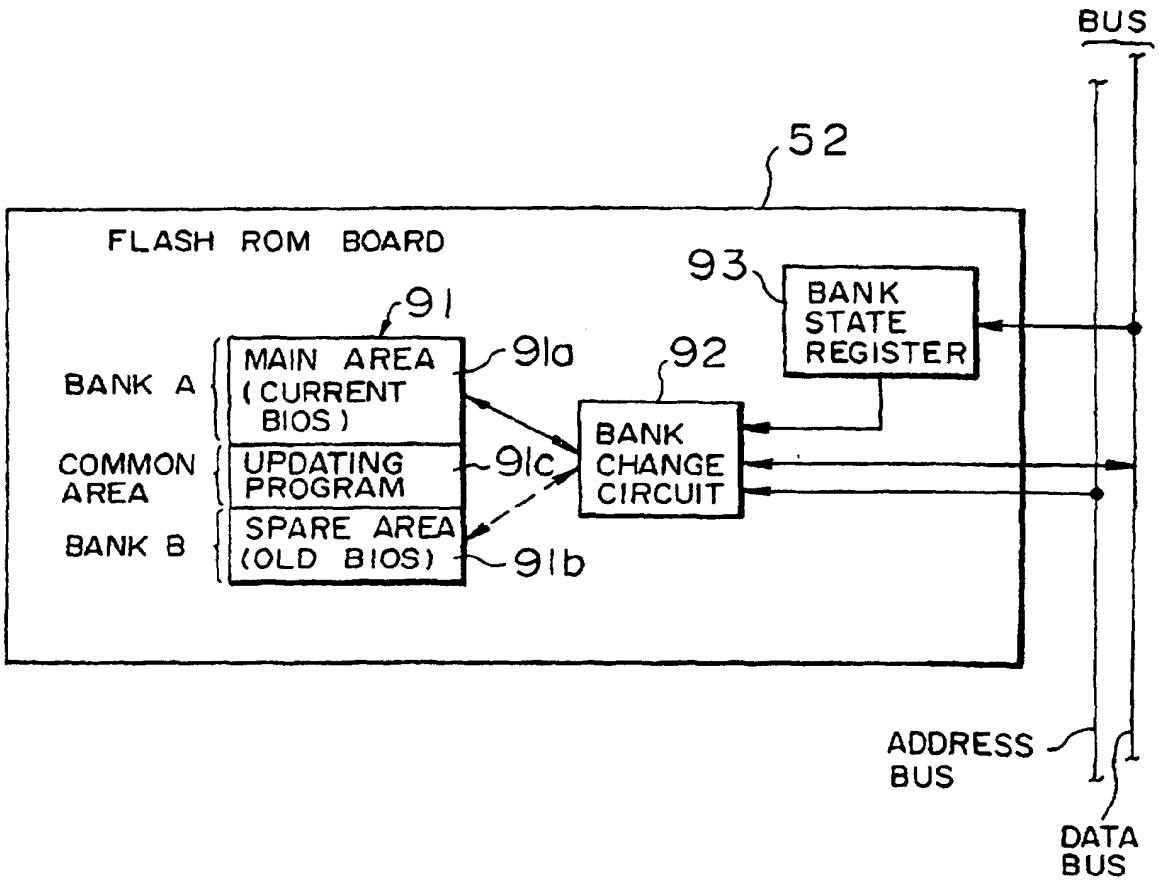

BUS
52
FLASH ROM BOARD
93
BANK STATE REGISTER
91
91a
92
BANK A
MAIN AREA (CURRENT BIOS)
BANK CHANGE CIRCUIT
COMMON AREA
UPDATING PROGRAM
91c
BANK B
SPARE AREA (OLD BIOS)
91b
ADDRESS BUS
DATA BUS

FIG. 7A

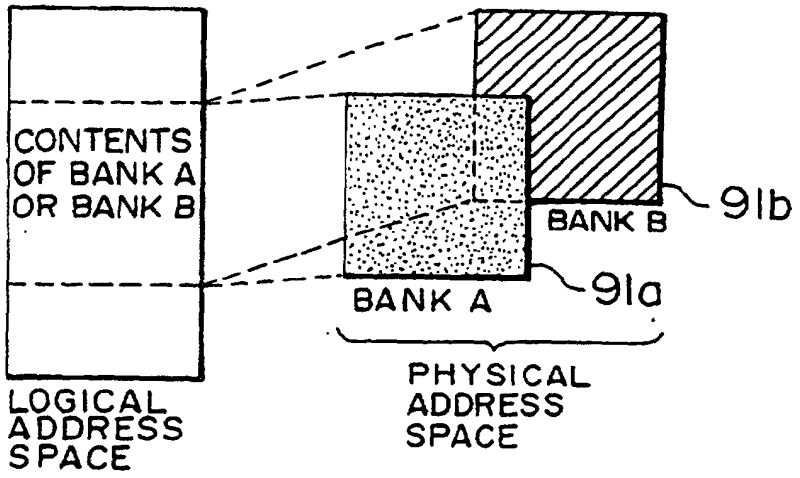


FIG. 7B

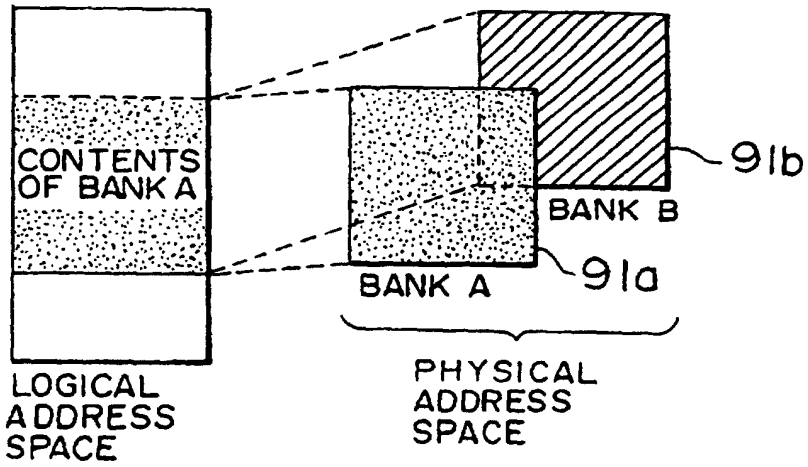


FIG. 7C

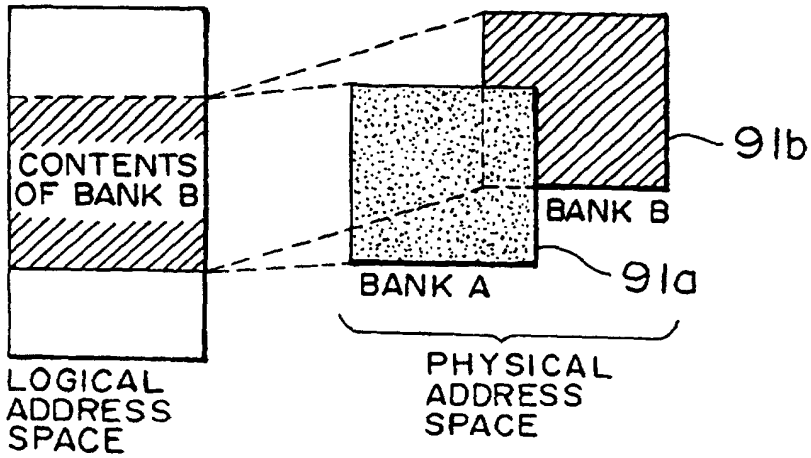


FIG. 8

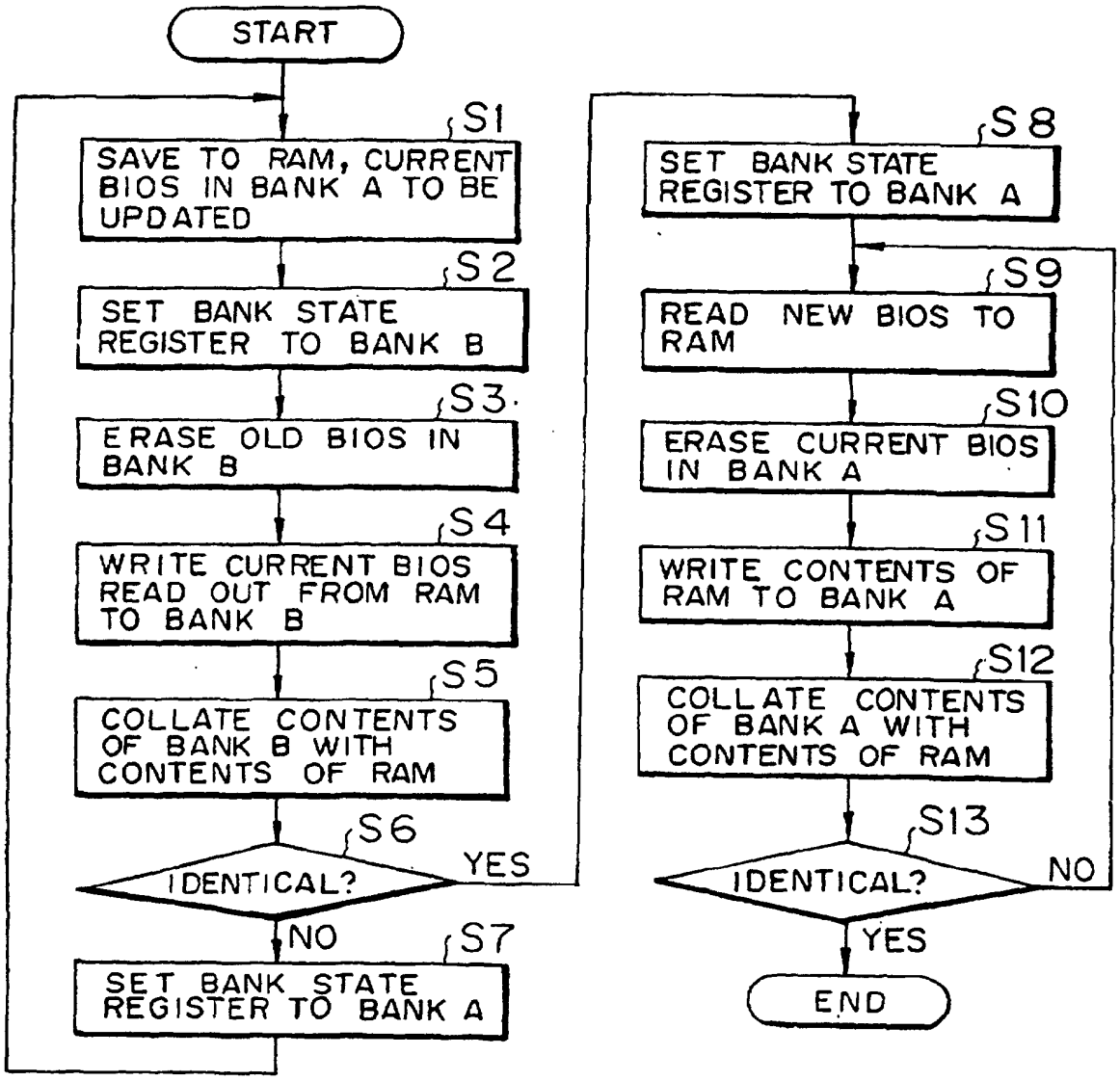

START
S1
SAVE TO RAM, CURRENT BIOS IN BANK A TO BE UPDATED
S2
SET BANK STATE REGISTER TO BANK B
S3
ERASE OLD BIOS IN BANK B
S4
WRITE CURRENT BIOS READ OUT FROM RAM TO BANK B
S5
COLLATE CONTENTS OF BANK B WITH CONTENTS OF RAM
S6
IDENTICAL?
YES
NO
S7
SET BANK STATE REGISTER TO BANK A
S8
SET BANK STATE REGISTER TO BANK A
S9
READ NEW BIOS TO RAM
S10
ERASE CURRENT BIOS IN BANK A
S11
WRITE CONTENTS OF RAM TO BANK A
S12
COLLATE CONTENTS OF BANK A WITH CONTENTS OF RAM
S13
IDENTICAL?
NO
YES
END

FIG. 9

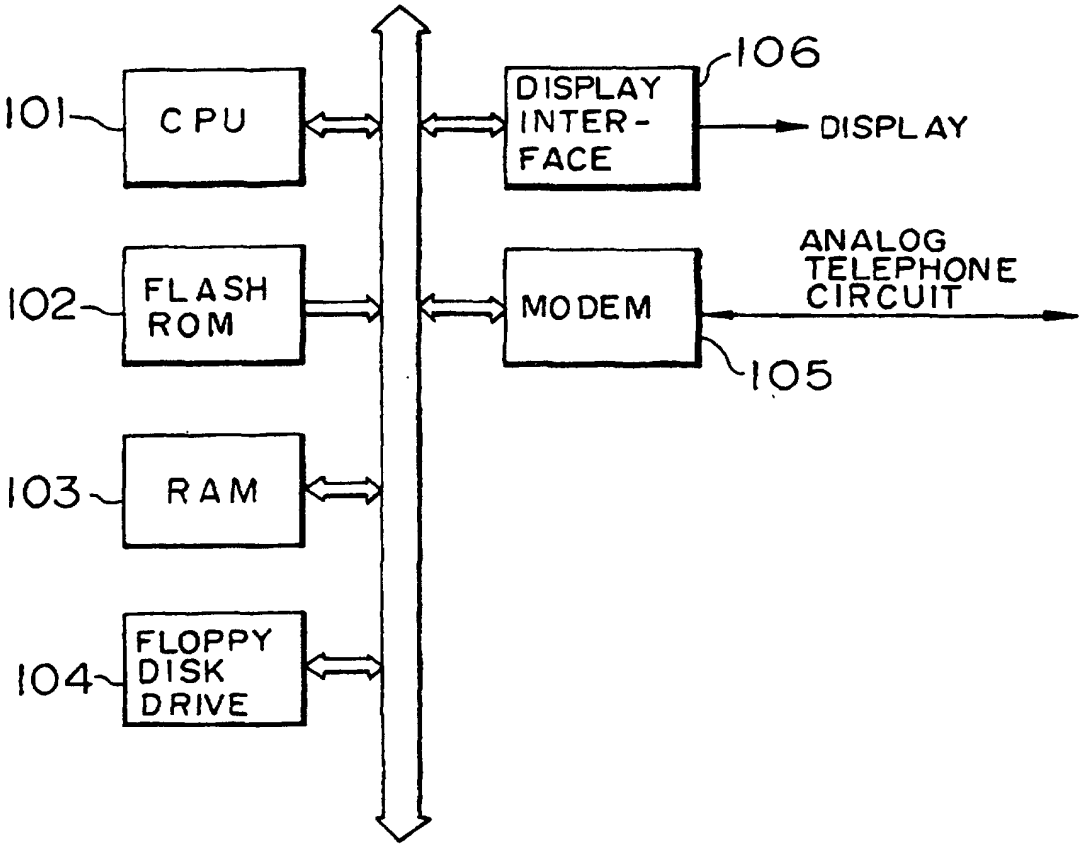

101
CPU
102
FLASH ROM
103
RAM
104
FLOPPY DISK DRIVE
DISPLAY INTER-FACE
106
DISPLAY
MODEM
105
ANALOG TELEPHONE CIRCUIT

FIG. 10

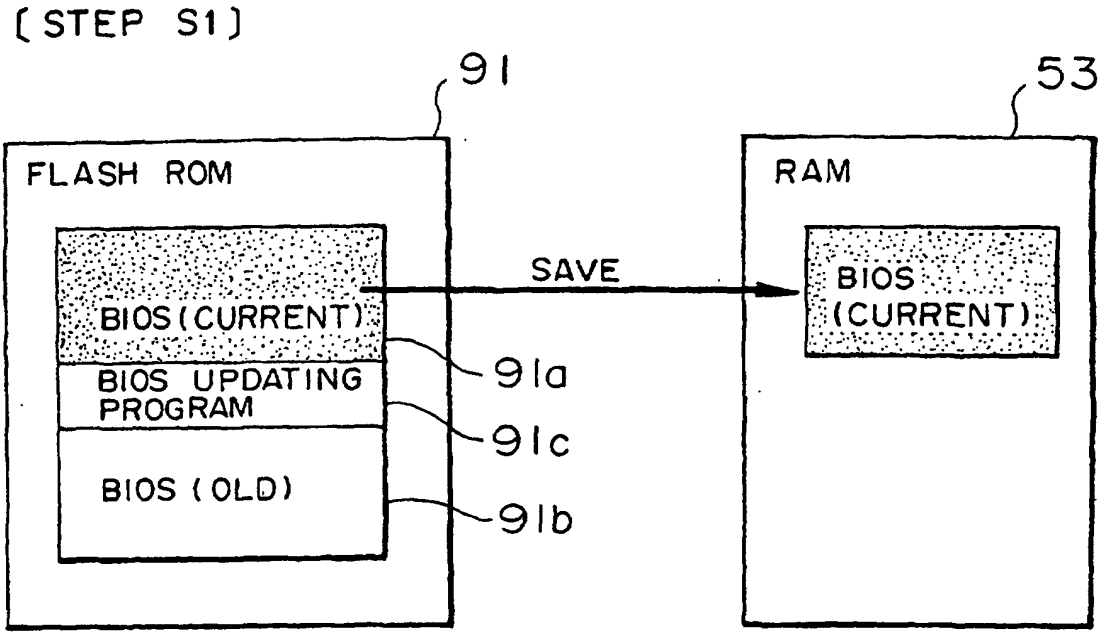

[STEP S1]
91
53
FLASH ROM
RAM
BIOS (CURRENT)
SAVE
BIOS (CURRENT)
BIOS UPDATING PROGRAM
BIOS (OLD)
91a
91c
91b

FIG. 11

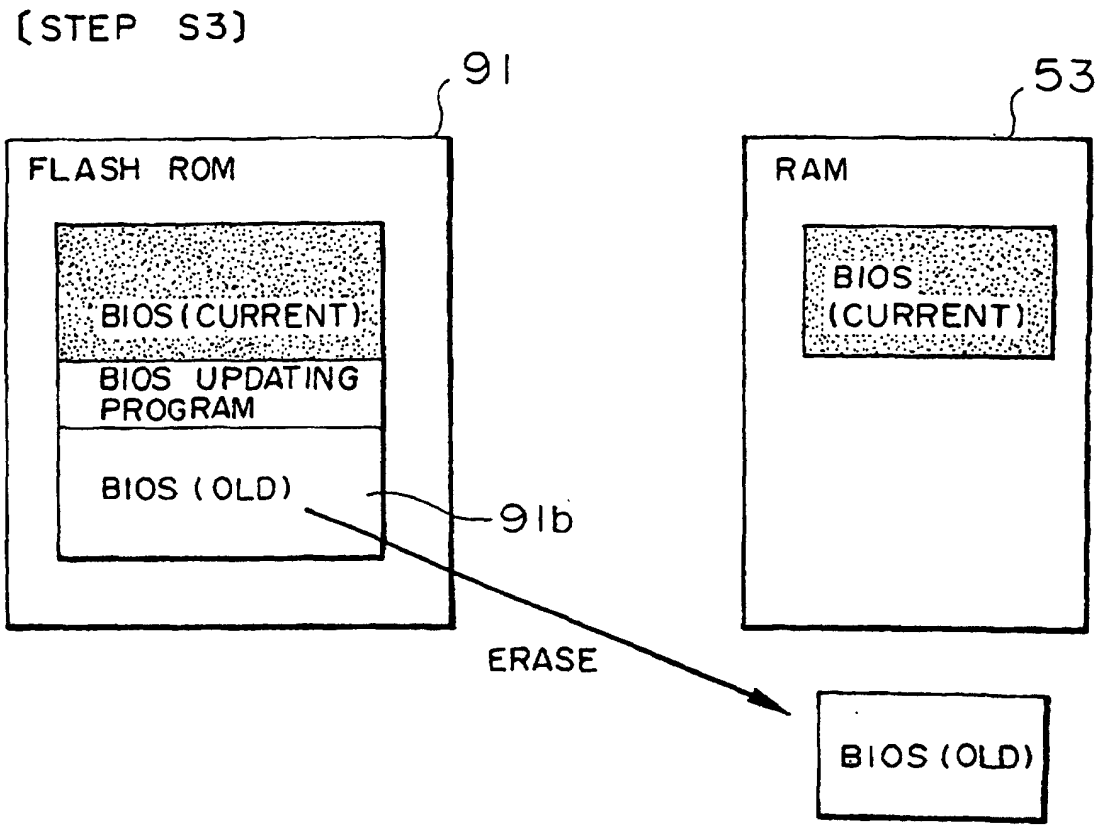

[STEP S3]
91
53
FLASH ROM
BIOS (CURRENT)
BIOS UPDATING PROGRAM
BIOS (OLD)
91b
RAM
BIOS (CURRENT)
ERASE
BIOS (OLD)

FIG. 12

[STEP S4]

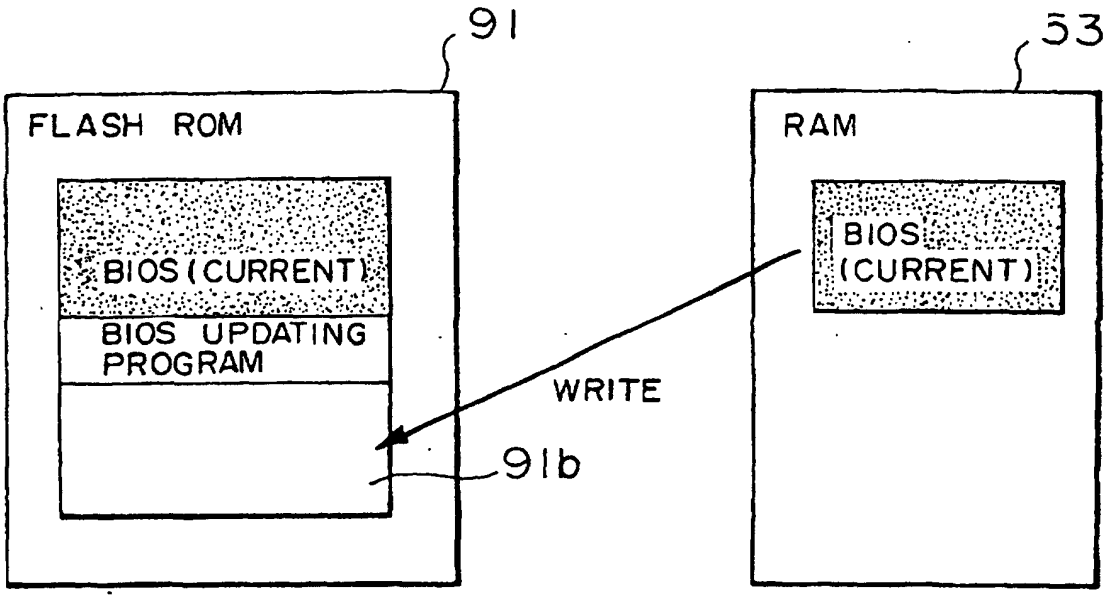


FIG. 13

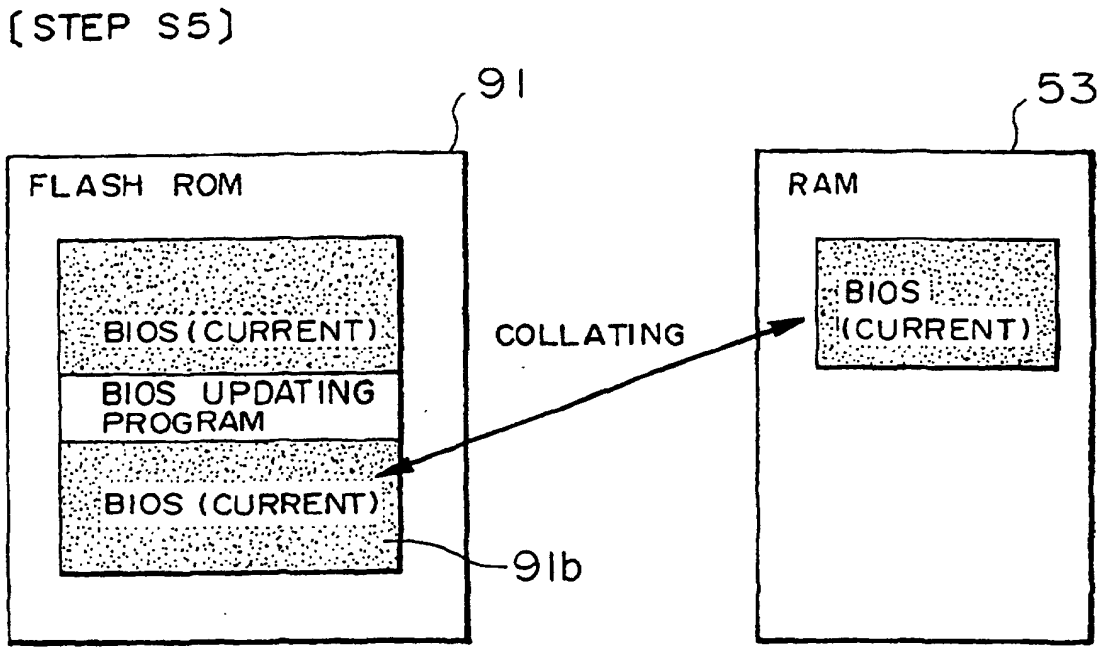

[STEP S5]
91
53
FLASH ROM
BIOS (CURRENT)
BIOS UPDATING PROGRAM
BIOS (CURRENT)
91b
COLLATING
RAM
BIOS (CURRENT)

FIG. 14

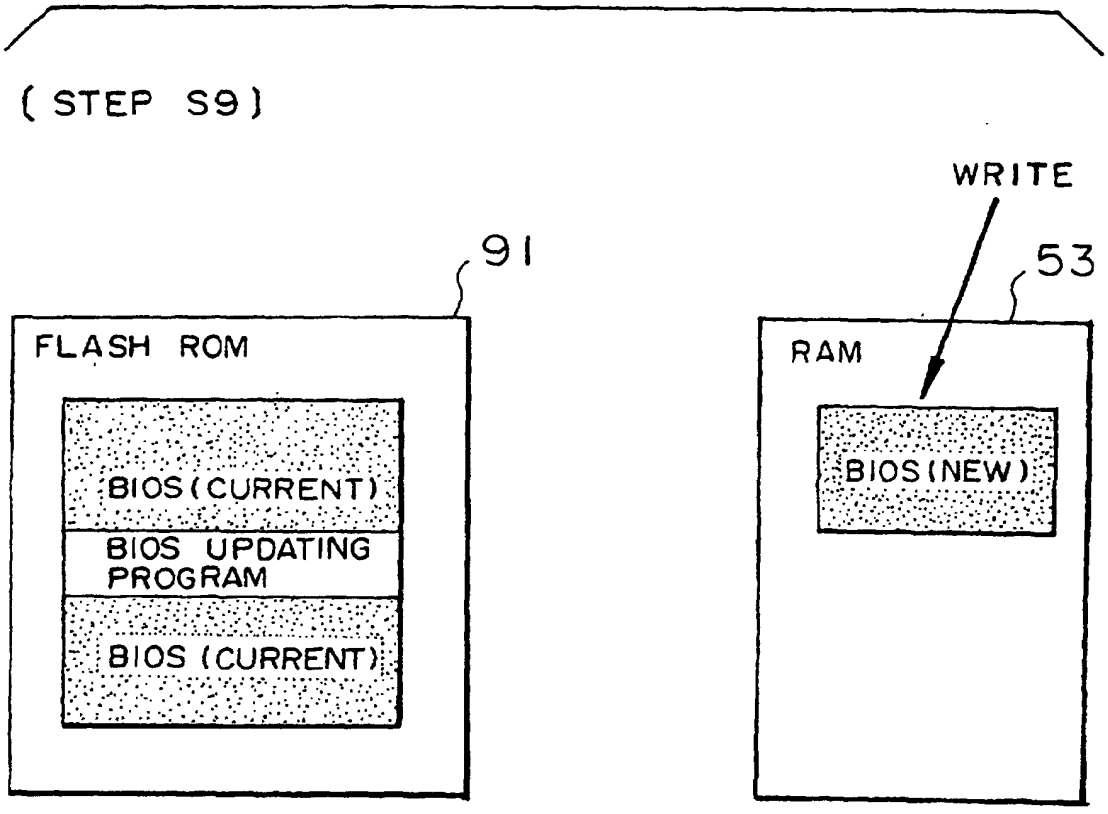

(STEP S9)
WRITE
91
53
FLASH ROM
BIOS(CURRENT)
BIOS UPDATING PROGRAM
BIOS (CURRENT)
RAM
BIOS(NEW)

FIG. 15

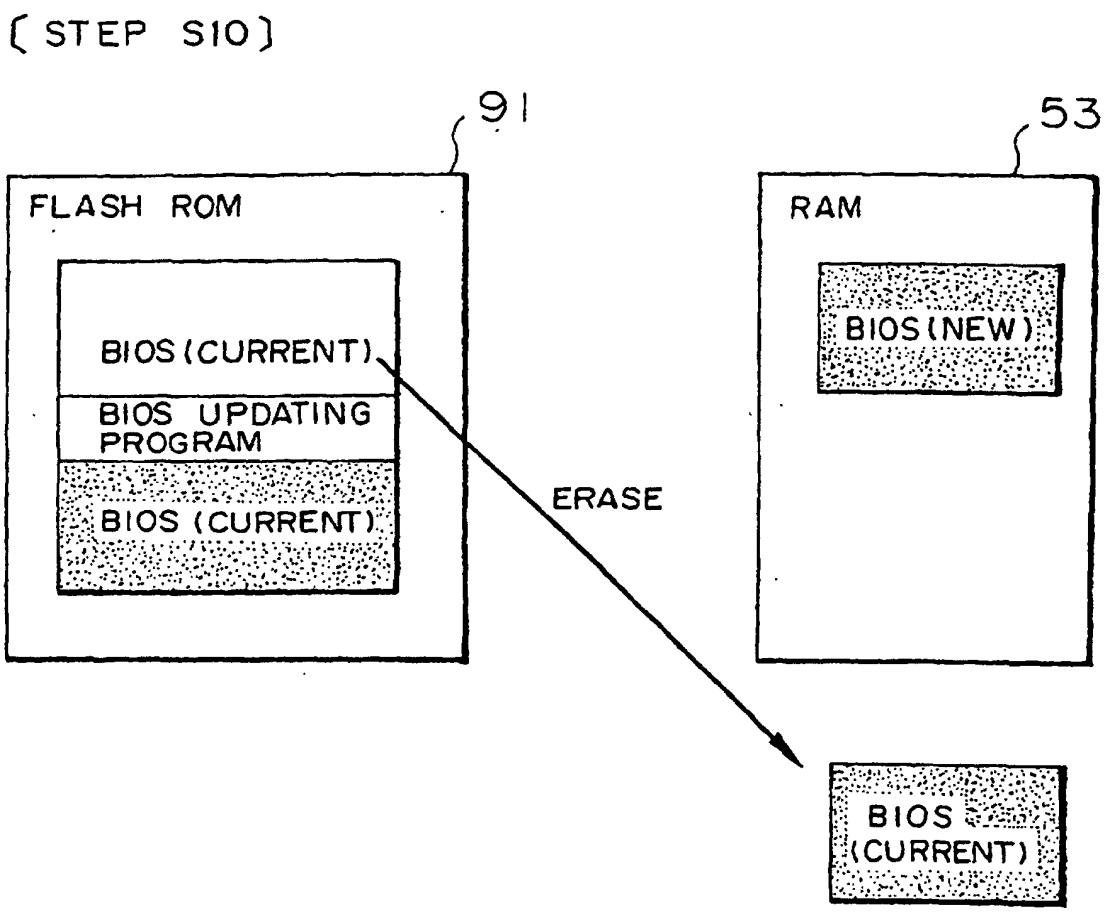

[STEP S10]
91
53
FLASH ROM
BIOS (CURRENT)
BIOS UPDATING PROGRAM
BIOS (CURRENT)
RAM
BIOS (NEW)
ERASE
BIOS (CURRENT)

FIG. 16

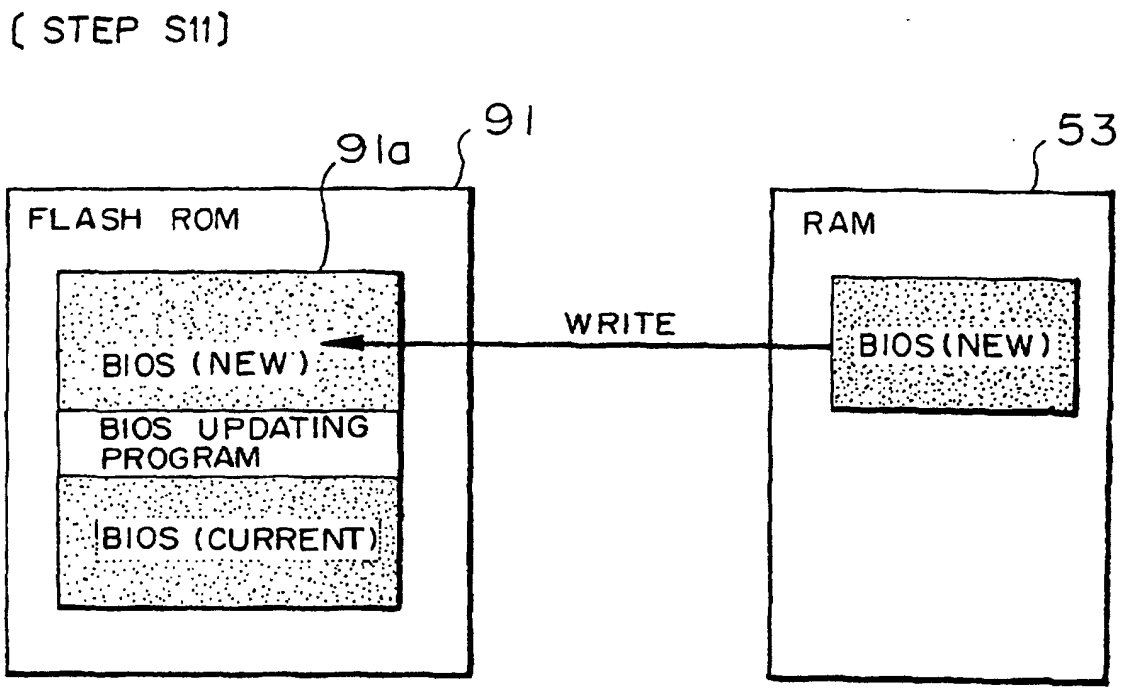

[STEP S11]
91a
91
53
FLASH ROM
RAM
BIOS (NEW)
BIOS UPDATING PROGRAM
BIOS (CURRENT)
WRITE
BIOS(NEW)

FIG. 17

[STEP S12]

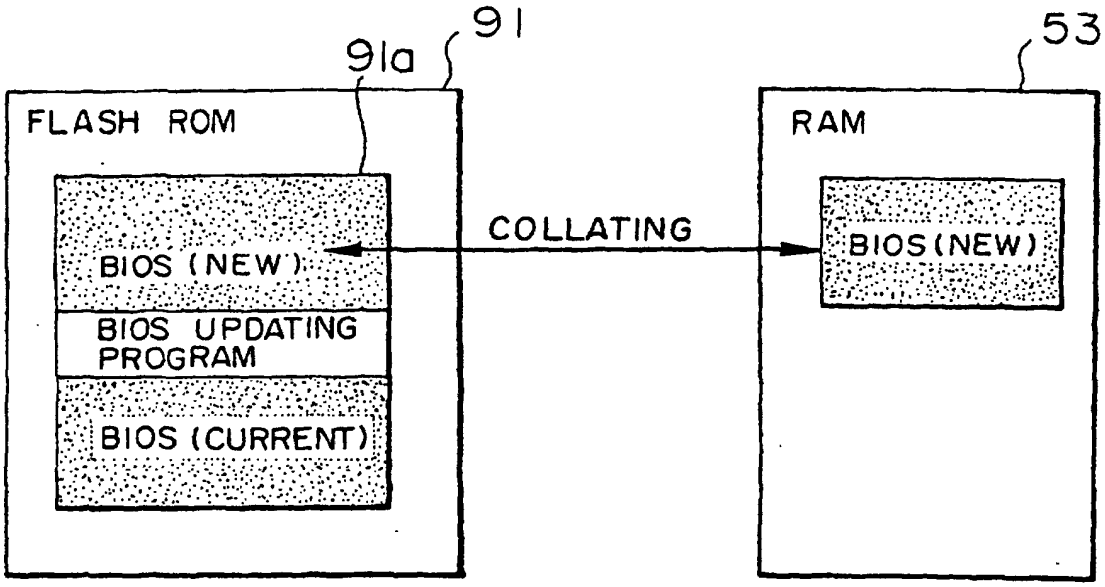
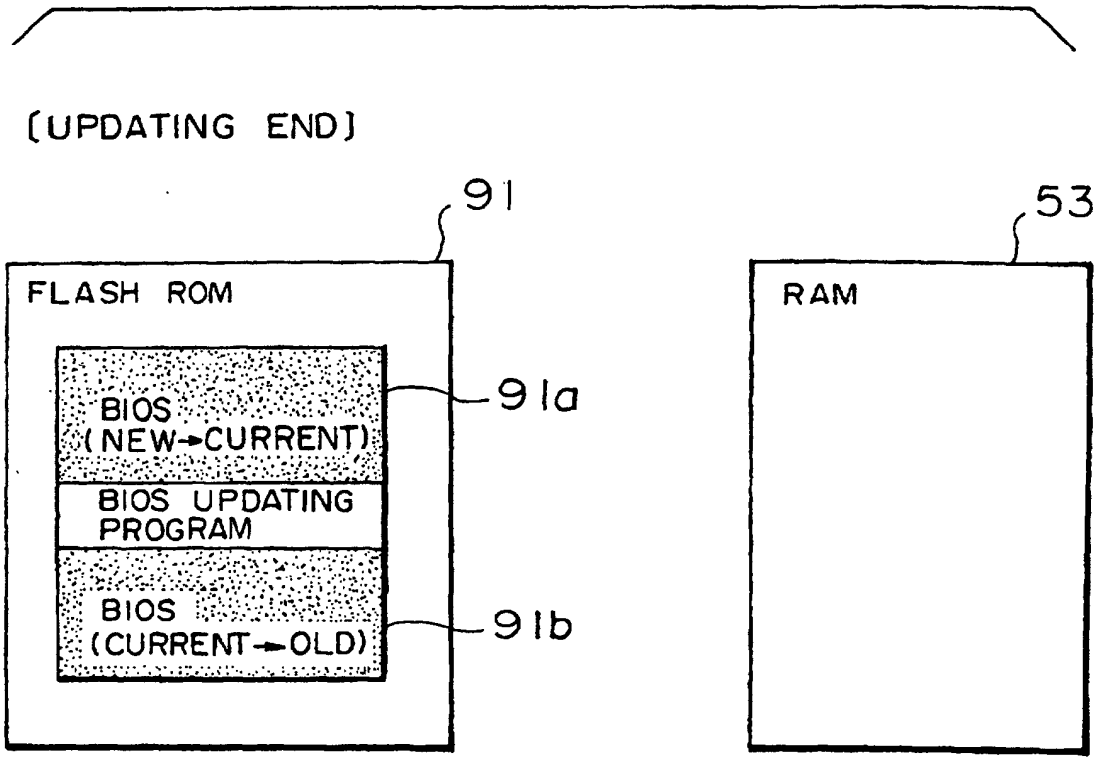


FIG. 18


(UPDATING END)
91
FLASH ROM
BIOS (NEW→CURRENT)
BIOS UPDATING PROGRAM
BIOS (CURRENT→OLD)
91a
91b
53
RAM